National Semiconductor

March 2006

LM27212
Two-Phase Current-Mode Hysteretic Buck Controller

General Description

The LM27212 is a two-phase synchronous buck regulator controller that is designed to support high-current loads such as microprocessors.

The IC employs a two-phase current-mode hysteretic control mechanism. During normal operation, the two switching channels operate 180˚ out of phase, helping reduce the number of input capacitors.

Inductor currents are sensed through low value sense resistors. Current sharing between the two channels is automatically guaranteed by multiplexing the feedback comparator.

The regulator input voltage range supported by the LM27212 is 5V to 30V. The output voltage is programmed through six voltage identification pins and ranges from 0.700V to 1.708V in 64 steps.

The IC provides accurate load-line characteristic. The regulator can be programmed to lower its output voltage linearly with increasing load current, so that the power generated by the load can be significantly reduced.

Since the error in the output voltage directly sets the inductor currents, the dynamic response to a large and fast load transient is close to a square wave. This is optimal for meeting CPU supply voltage specifications.

Due to the intrinsic input voltage feed forward characteristic of a peak current-mode controller, the IC has a superior line transient response.

The IC provides a cycle-by-cycle peak current limit, overvoltage protection, and a power good signal.

The LM27212 fully supports the Stop CPU mode and Sleep mode required by some mobile CPUs. In the Sleep mode, the IC enters single-phase power-saving operation which significantly enhances the light load efficiency.

The LM27212 also has a soft start pin for the external adjustment of soft start speed.

The LM27212 combined with the LM27222 series of MOSFET drivers, provides a layout-friendly, thermally optimized and noise-immune power solution for the mobile platform.

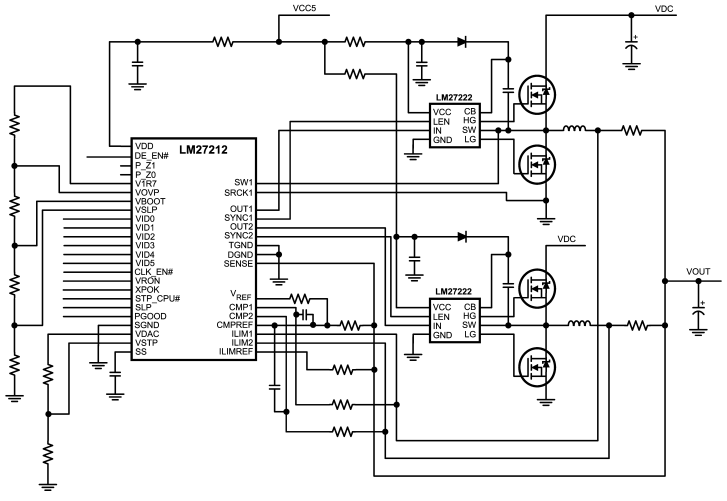
Features

- 5V to 30V input range
- Two channels operating 180˚ out of phase
- Ideal load and line transient responses
- Dynamic output voltage swing supported
- Excellent inductor current sharing
- High efficiency Sleep mode
- Soft start and soft shutdown
- Cycle-by-cycle current limit
- Adjustable over-voltage protection
- Accurate load-line supported
- ±1% reference over temperature
- On/off pin and power good signal
- TSSOP package or tiny LLP package

Applications

- Power Supply For Mobile CPUs
- Low Output Voltage Buck Regulators Up To 50A

Typical Application



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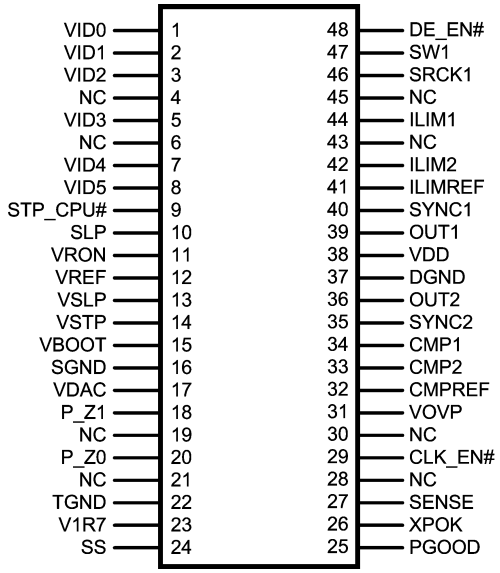
Connection Diagrams

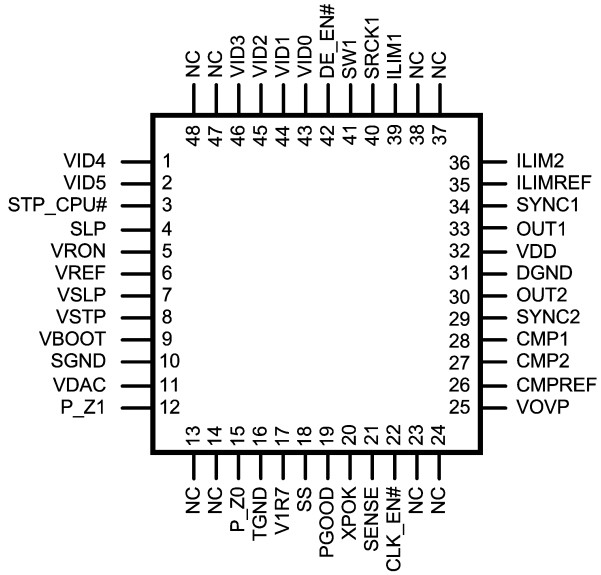
Top View



20152001

48-Lead TSSOP (MTD)
Order Number LM27212MTD
See NS Package Number MTD48

Top View



20152002

48-Lead LLP
Order Number LM27212SQ
NS Package Number SQA48A

Ordering Information

Order Number	Package Drawing	Supplied As
LM27212MTD	MTD48	38 Units/Rail
LM27212MTDX	MTD48	1000 Units Tape and Reel
LM27212SQ	SQA48A	1000 Units Tape and Reel
LM27212SQX	SQA48A	4500 Units Tape and Reel

Pin Descriptions (TSSOP)

Pin 1, VID0: First and least significant bit to program the output voltage, as specified in VID Code table.

Pin 2, VID1: 2nd bit to program the output voltage, as specified in VID Code table.

Pin 3, VID2: 3rd bit to program the output voltage, as specified in VID Code table.

Pin 4, NC: No connect.

Pin 5, VID3: 4th bit to program the output voltage, as specified in VID Code table.

Pin 6, NC: No connect.

Pin 7, VID4: 5th bit to program the output voltage, as specified in VID Code table.

Pin 8, VID5: 6th and most significant bit to program the output voltage, as specified in VID Code table.

Pin 9, STP_CPU#: When this pin is logic low, VREF voltage is equal to that on the VSTP pin. This pin offers the power supply designer a way to dynamically (meaning when the regulator is running) lower the output voltage by a preset percentage of the VREF value.

Pin 10, SLP: When this pin is logic high, VREF voltage is equal to that on the SLP pin. The pin offers the power supply designer a way to dynamically (meaning when the regulator is running) change the output voltage to a preset fixed value.

Pin 11, VRON: Chip enable input. When this pin goes high, soft start begins. When this pin goes low, soft shutdown begins.

Pin 12, VREF: Desired regulator output voltage under no load.

Pin 13, VSLP: Desired Sleep mode output voltage. Connect this pin to the desired reference level. See the typical application circuit. Also refer to the Pin 10 definition.

Pin 14, VSTP: Desired Stop CPU mode output voltage. Connect this pin to the desired reference level. See the typical application circuit. Also refer to the Pin 9 definition.

Pin 15, VBOOT: Initial output voltage desired after soft start completes. Connect this pin to the desired reference level. This pin offers the power supply designer a way to start into a different voltage than the final desired value. The output voltage will start slewing (in a controlled manner) to the value defined by the VID pins about 25µs after output voltage reaches VBOOT. See Timing Diagram.

Pin 16, SGND: Signal ground.

Pin 17, VDAC: Buffered Digital-to-Analog converter output.

Pins 18 P_Z1: Reference adjust, do not connect.

Pin 19, NC: No connect.

Pins 20 P_Z0: Reference adjust, do not connect.

Pin 21, NC: No connect.

Pin 22, TGND: Reserved for test purpose. Must be connected to signal ground.

Pin 23, V1R7: 1.7V reference voltage.

Pin 24, SS: Soft start, soft shutdown and slew rate control. Connect a capacitor between this pin and ground to control the soft start and soft shutdown speed. The value of the capacitor will also define the slew rate of the output voltage swings. There is an internal current source charging or discharging the capacitor at this pin. The current for soft start and soft shutdown is typically 22µA and 45µA respectively, and the current for dynamic output voltage swing (whether it is a Dynamic VID change or it is a change to or from Stop CPU or Sleep Mode) is typically 335µA.

Pin 25, PGOOD: Power good flag. Open-drain when output voltage enters the power good window and XPOK is asserted. Masked during dynamic output voltage transitions. See Timing Diagram for further details.

Pin 26, XPOK: Power good control. Only when this pin is a logic high can PGOOD pin be pulled high. Connect this pin to the power good flag of another regulator if the latter needs to be powered up first.

Pin 27, SENSE: Regulator output voltage sense. Connect directly to output.

Pin 28, NC: No connect.

Pin 29, CLK_EN#: An output signal provided as a convenience to enable an external logic circuit if needed. It is asserted typically 18µs after both XPOK is high and the output voltage is within power good window.

Pin 30, NC: No connect.

Pin 31, VOVP: Over-voltage protection level. Connect this pin to the desired reference voltage to set the trigger level for over-voltage protection.

Pins 32, CMPREF: Inductor current reference. Voltage between this pin and the regulator output determines the inductor current.

Pin 33, CMP2: Current sense for Channel 2. Voltage between this pin and the regulator output is compared with the voltage between inductor current reference (Pin 32) and the regulator output to control the inductor current.

Pin 34, CMP1: Current sense for Channel 1. Voltage between this pin and the regulator output is compared with the voltage between inductor current reference (Pin 32) and the regulator output to control the inductor current.

Pin 35, SYNC2: Connect to the LEN pin of the LM27222 driver to enable or disable the turning on of the bottom power FET.

Pin 36, OUT2: Channel 2 pulse output to control the switching of the external MOSFET driver such as the LM27222.

Pin 37, DGND: Digital ground.

Pin 38, VDD: Chip power supply.

Pin 39, OUT1: Channel 1 pulse output to control the switching of the external MOSFET driver such as the LM27222.

Pin 40, SYNC1: Connect to the LEN pin of the LM27222 driver to enable or disable the turning on of the low-side power FET.

Pin 41, ILIMREF: Current limit reference. Voltage between this pin and the regulator output sets the inductor current limit level.

Pin 42, ILIM2: Current limit sense for Channel 2. Voltage between this pin and the regulator output is the voltage across the current sense resistor.

Pin 43, NC: No connect.

Pin 44, ILIM1: Current limit sense for Channel 1. Voltage between this pin and the regulator output is the voltage across the current sense resistor.

Pin 45, NC: No connect.

Pin 46, SRCK1: Kelvin connect to Channel 1 bottom FET source node (ground) to detect negative inductor current.

Pin 47, SW1: Connect to Channel 1 switch node (drain of low-side power FET) to detect negative inductor current.

Pin 48, DE_EN#: Diode emulator mode trigger signal. When the IC is in Sleep mode, if this pin is logic low, the regulator will shut down Channel 2 and force Channel 1 to run in diode emulation mode (bottom FET is turned off when inductor current goes negative).

Pin Descriptions (LLP)

Pin 1, VID4: 5th bit to program the output voltage, as specified in VID Code table.

Pin 2, VID5: 6th and most significant bit to program the output voltage, as specified in VID Code table.

Pin 3, STP_CPU#: When this pin is logic low, VREF voltage is equal to that on the VSTP pin. This pin offers the power supply. designer a way to dynamically (meaning when the regulator is running) lower the output voltage by a preset percentage of the VREF value.

Pin 4, SLP: When this pin is logic high, VREF voltage is equal to that on the VSLP pin. The pin offers the power supply designer a way to dynamically (meaning when the regulator is running) change the output voltage to a preset fixed value.

Pin 5, VRON: Chip enable input. When this pin goes high, soft start begins. When this pin goes low, soft shutdown begins.

Pin 6, VREF: Desired regulator output voltage under no load.

Pin 7, VSLP: Desired Sleep mode output voltage. Connect this pin to the desired reference level. See the typical application circuit. Also refer to the Pin 4 definition.

Pin 8, VSTP: Desired Stop CPU mode output voltage. Connect this pin to the desired reference level. See the typical application circuit. Also refer to the Pin 3 definition.

Pin 9, VBOOT: Initial output voltage desired after soft start completes. Connect this pin to the desired reference level. This pin offers the power supply designer a way to start into a different voltage than the final desired value. The output voltage will start slewing (in a controlled manner) to the value defined by the VID pins about 25µs after output voltage reaches VBOOT. See Timing Diagram.

Pin 10, SGND: Signal ground.

Pin 11, VDAC: Buffered Digital-to-Analog converter output.

Pins 12, P_Z1: Reference adjust, do not connect.

Pins 13, NC: No connect.

Pins 14, NC: No connect.

Pins 15, P_Z0: Reference adjust, do not connect.

Pin 16, TGND: Reserved for test purpose. Must be connected to signal ground.

Pin 17, V1R7: 1.7V reference voltage.

Pin 18, SS: Soft start, soft shutdown and slew rate control. Connect a capacitor between this pin and ground to control the soft start and soft shutdown speed. The value of the capacitor will also define the slew rate of the output voltage swings. There is an internal current source charging or discharging the capacitor at this pin. The current for soft start and soft shutdown is typically 22µA and 45µA respectively, and the current for dynamic output voltage swing (whether it is a Dynamic VID change or it is a change to or from Stop CPU or Sleep mode) is typically 335µA.

Pin 19, PGOOD: Power good flag. Goes open-drain when output voltage enters the power good window and XPOK is asserted. Masked during dynamic output voltage transitions. See Timing Diagram for further details.

Pin 20, XPOK: Power good control. Only when this pin is a logic high can PGOOD pin be pulled high. Connect this pin to the power good flag of another regulator if the latter needs to be powered up first.

Pin 21, SENSE: Regulator output voltage sense. Connect directly to output.

Pin 22, CLK_EN#: An output signal provided as a convenience to enable an external logic circuit if needed. It is asserted typically 18µs after both XPOK is high and output voltage is within power good window.

Pin 23, NC: No connect.

Pin 24, NC: No connect.

Pin 25, VOVP: Over-voltage protection level. Connect this pin to the desired reference voltage to set the trigger level for over-voltage protection.

Pins 26, CMPREF: Inductor current reference. Voltage between this pin and the regulator output determines the inductor current.

Pin 27, CMP2: Current sense for Channel 2. Voltage between this pin and the regulator output is compared with the voltage between the inductor current reference (Pin 26) and the regulator output to control the inductor current.

Pin 28, CMP1: Current sense for Channel 1. Voltage between this pin and the regulator output is compared with the voltage betwen inductor current reference (Pin 26) and the regulator output to control the inductor current.

Pin 29, SYNC2: Connect to the LEN pin of the LM27222 driver to enable or disable the turning on of the bottom power FET.

Pin 30, OUT2: Channel 2 pulse output to control the switching of the external MOSFET driver such as the LM27222.

Pin 31, DGND: Digital ground.

Pin 32, VDD: Chip power supply.

Pin 33, OUT1: Channel 1 pulse output to control the switching of the external MOSFET driver such as the LM27222.

Pin 34, SYNC1: Connect to the LEN pin of the LM27222 driver to enable or disable the turning on of the bottom power FET.

Pin 35, ILIMREF: Current limit reference. Voltage between this pin and the regulator output sets the inductor current limit level.

Pin 36, ILIM2: Current limit sense for Channel 2. Voltage between this pin and the regulator output is the voltage across the current sense resistor.

Pins 37, NC: No connect.

Pins 38, NC: No connect.

Pin 39, ILIM1: Current limit sense for Channel 1. Voltage between this pin and the regulator output is the voltage across the current sense resistor.

Pin 40, SRCK1: Kelvin connect to Channel 1 bottom FET source node (ground) to detect negative inductor current.

Pin 41, SW1: Connect to Channel 1 switch node (drain of bottom power FET) to detect negative inductor current.

Pin 42, DE_EN#: Diode emulator mode trigger signal. When the IC is in Sleep mode, if this pin goes low, the regulator will shut down Channel 2 and force Channel 1 to run in diode emulation mode (bottom FET is turned off when inductor current goes negative).

Pin 43, VID0: First and least significant bit to program the output voltage, as specified in VID Code table.

Pin 44, VID1: 2nd bit to program the output voltage, as specified in VID Code table.

Pin 45, VID2: 3rd bit to program the output voltage, as specified in VID Code table.

Pin 46, VID3: 4th bit to program the output voltage, as specified in VID Code table.

Pins 47 & 48, NC: No connect.

VID Code Table

VID						Voltage	VID						Voltage
5	4	3	2	1	0	(V)	5	4	3	2	1	0	(V)
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VDD	-0.6V to 7V
XPOK	-0.6V to 7V
SW1	-3V to 32V
VRON	-0.6V to 7V
DE_EN#	-0.6V to 7V
VOVP, VBOOT	-0.6V to 7V
VID0 to VID5	-0.6V to 7V
STP_CPU#, SLP	-0.6V to 7V
VSLP, VSTP, SENSE	-0.6V to 7V
CMP1, CMP2, CMPREF	-0.6V to 7V
ILIM1, ILIM21, ILIMREF	-0.6V to 7V
Power Dissipation \TSSOP, TA = 25˚C, (Note 2)	1.56W
Junction Temperature	+150˚C
Functional Temp. Range (Note 1)	-20˚C to +110˚C
ESD Rating (Note 4)	2kV
Storage Temp Range (Note 3)	-65˚C to +150˚C
Soldering Dwell Time Temperature (Note 3)	
Wave	4sec, 260˚C
Infrared	10sec, 240˚C
Vapor Phase	75sec, 219˚C

Operating Ratings (Note 1)

VDD	4.75V to 6V
Junction Temperature	-5˚C to +110˚C
Ambient Temperature	-5˚C to +105˚C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those in **bold face type** apply over a junction temperature range of -5˚C to +110˚C. Unless otherwise specified, VDD = 5V, SGND = DGND = SRCK1 = 0V. (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Chip Supply						
	VDD Shutdown Current	VRON = 0V, VDD = 6V.		1	**10**	µA
	VDD Normal Operating Current	VRON = 3.3V.		3	**4.2**	mA
	UVLO Threshold	VDD goes high from 0V.	**3.9**	4.1	**4.3**	V
	UVLO Hysteresis	VDD falls from above UVLO Threshold.	**0.2**	0.35		V
Logic						
	VRON, STP_CPU#, XPOK and SLP Input Logic Low-to-High Transition Threshold	VRON, STP_CPU#, XPOK or SLP go high from 0V.		1.9	**2.31**	V
	VRON, STP_CPU#, XPOK and SLP Input Logic High-to-Low Transition Threshold	VRON, STP_CPU#, XPOK or SLP fall from 3.3V.	**0.99**	1.43		V
	CLK_EN# Sink Current	CLK_EN# = 0.1V and asserted.	**2**	3.2		mA
Power Good						
	Power Good Upper Threshold As a Percentage of VREF	SENSE voltage goes high from 0V.	**108**	112	**116**	%
	Power Good Lower Threshold As a Percentage of VREF	SENSE voltage falling from above VREF.	**84.5**	87	**90.5**	%
	Hysteresis			2		%
	Power Good Delay			3.6		µs
	PGOOD Sink Current	PGOOD = 0.1V and asserted.	**2**	3		mA
Output Voltage Slew Rate Control						
I_{SS1}	SS Pin Charging Current During Soft Start	SS = 0V.	**16**	22	**32**	µA
I_{SS2}	SS Pin Discharging Current During Soft Shutdown		**33**	45	**57**	µA

Electrical Characteristics Specifications with standard typeface are for T_J = 25˚C, and those in **bold face type** apply over a junction temperature range of -5˚C to +110˚C. Unless otherwise specified, VDD = 5V, SGND = DGND = SRCK1 = 0V. (Note 5) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{SS3}	Dynamic Output Swing Slew Rate Control Current (charging)		**255**	335	**415**	µA
DAC and References						
	VID Pins Input Logic Low-to-High Transition Threshold				**0.63**	V
	VID Pins Input Logic High-to-Low Transition Threshold		**0.315**			V
	DAC Accuracy Measured at VREF Pin.	-5˚C < Tj < 85˚C				
		DAC codes from 0.844V to 1.708V.	**-1.0**		**+1.0**	%
		DAC codes from 0.700V to 0.828V.	**-1.3**		**+1.3**	%
		-5˚C < Tj < 110˚C				
		DAC codes from 0.844V to 1.708V.	**-1.3**		**+1.3**	%
		DAC codes from 0.700V to 0.828V.	**-1.5**		**+1.5**	%
	V1R7 Accuracy	17kΩ from V1R7 to GND.	**1.674**	1.708	**1.742**	V
	VSTP Offset	VSTP = 1.398V, Measured at VREF pin.	**-4.5**		**+4.5**	mV
	VBOOT Offset	VBOOT = 1.00V, Measured at VREF pin.	**-4.5**		**+4.5**	mV
	VSLP Offset	VSLP = 0.748V, Measured at VREF pin.	**-4.5**		**+4.5**	mV
	VREF Driving Capability	source		1.5		mA
		sink		11.7		mA
	VDAC Driving Capability	source		1.4		mA
		sink		14.3		mA
	V1R7 Driving Capability	source	**90**	580		µA
Error Comparator						
	Error Comparator Input Bias Current (Sourcing)	CMP1 = CMP2 = 1.436V.	**12**	21	**38**	µA
	Error Comparator Input Offset Voltage	CMPREF = 1.436V.	**-2**		**+2**	mV
	Hysteresis Current	Rhys = 17kΩ	**82**	98	**115**	µA
		Rhys = 170kΩ		10		µA
	Error Comparator Propagation Delay	20mV overdrive		70		ns
Current Limit						
	Current Limit Comparator Input Bias Current		**9**	21	**35**	µA
	Current Limit Comparator Input Offset Voltage	ILIMREF = 1.436V.	**-2**		**+2**	mV
	Current Limit Setting Current	Rhys = 17kΩ, ILIMREF < ILIMx	**255**	294	**345**	µA
		Rhys = 17kΩ, ILIMREF > ILIMx		250		µA
		Rhys = 170kΩ, ILIMREF < ILIMx		30		µA
Time Delays						
t_{BOOT}	VBOOT Voltage Holdup Time	From assertion of XPOK to assertion of CLK_EN#.	**10**	18	**30**	µs
t_{CPU_PWRGD}	Power Good Mask For Initial VID Voltage Settling During Start Up	From assertion of CLK_EN# to assertion of PGOOD.	**3**	5	**9**	ms

Electrical Characteristics Specifications with standard typeface are for T_J = 25˚C, and those in **bold face type** apply over a junction temperature range of -5˚C to +110˚C. Unless otherwise specified, VDD = 5V, SGND = DGND = SRCK1 = 0V. (Note 5) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Good Mask For Dynamic Output Swing		**100**	133	**179**	µs
	Power Good De-assertion Delay Upon Shutdown	Delay From VRON de-assertion to PGOOD de-assertion		90		ns
Over-voltage Protection						
	SENSE Voltage as a Percentage of VOVP	VOVP = VREF	**109**	123	**139**	%
System						
	DE_EN# Input Logic Low-to-High Transition Threshold				**0.63**	V
	DE_EN# Input Logic High-to-Low Transition Threshold		**0.315**			V
	DE_EN# Pin Leakage Current	DE_EN# = 7.5V			**100**	µA
	Soft Shutdown Finish Threshold			0.3		V

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics table. Functional temperature range is the range within which the device performs its intended functions, but not necessarily meeting the limits specified in the Electrical Characteristic table.

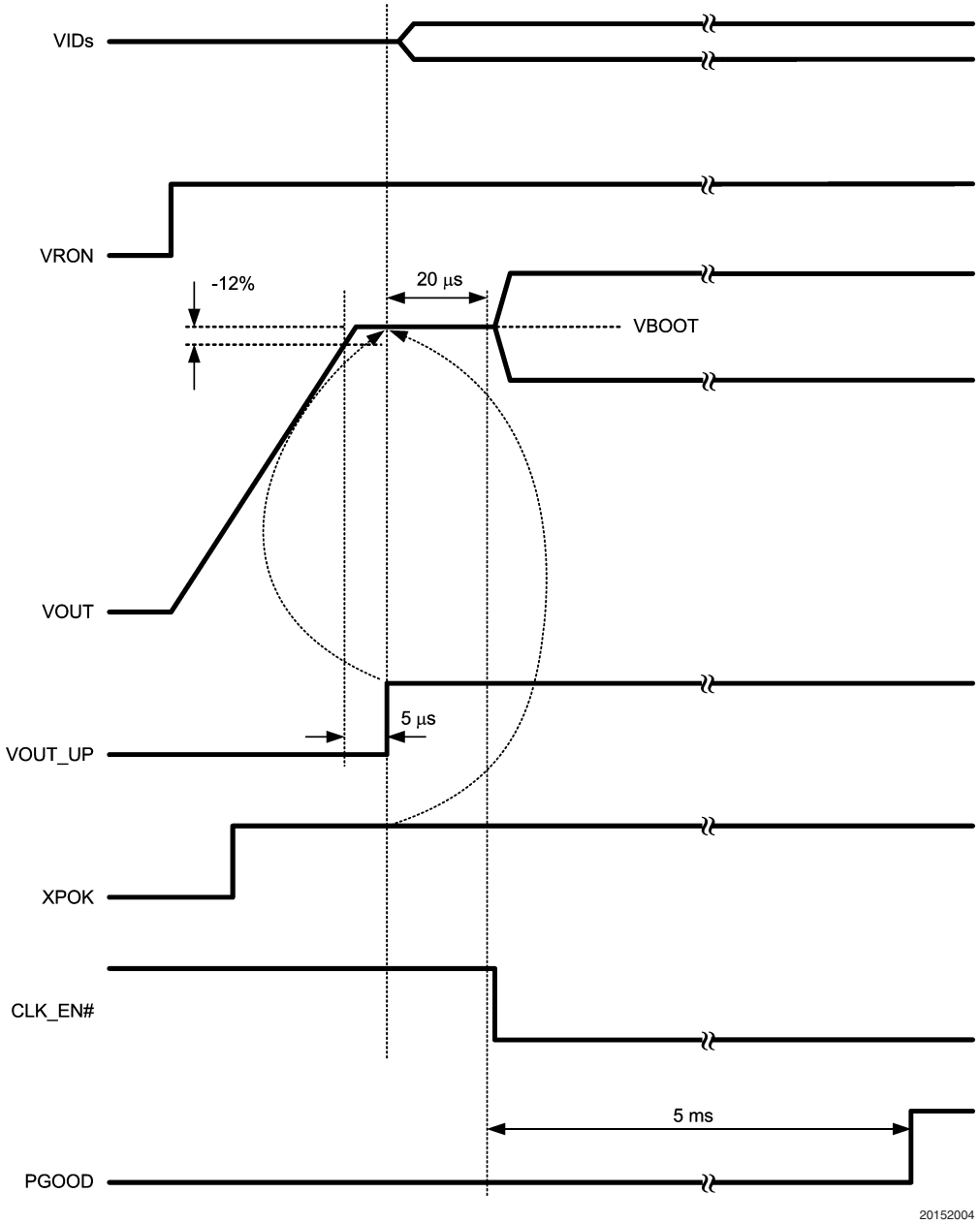
Note 2: The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{JMAX} - T_A) / \theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 1.56W rating results from using 150˚C, 25˚C, and 80˚C/W for T_{JMAX}, T_A, and θ_{JA} respectively. The θ_{JA} of 90˚C/W represents the worst-case condition with no heat sinking of the 48-Pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation should be de-rated by 12.5mW per ˚C above 25˚C ambient. The LM27212 actively limits its junction temperature to about 150˚C.

Note 3: For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook available from National Semiconductor Corporation.

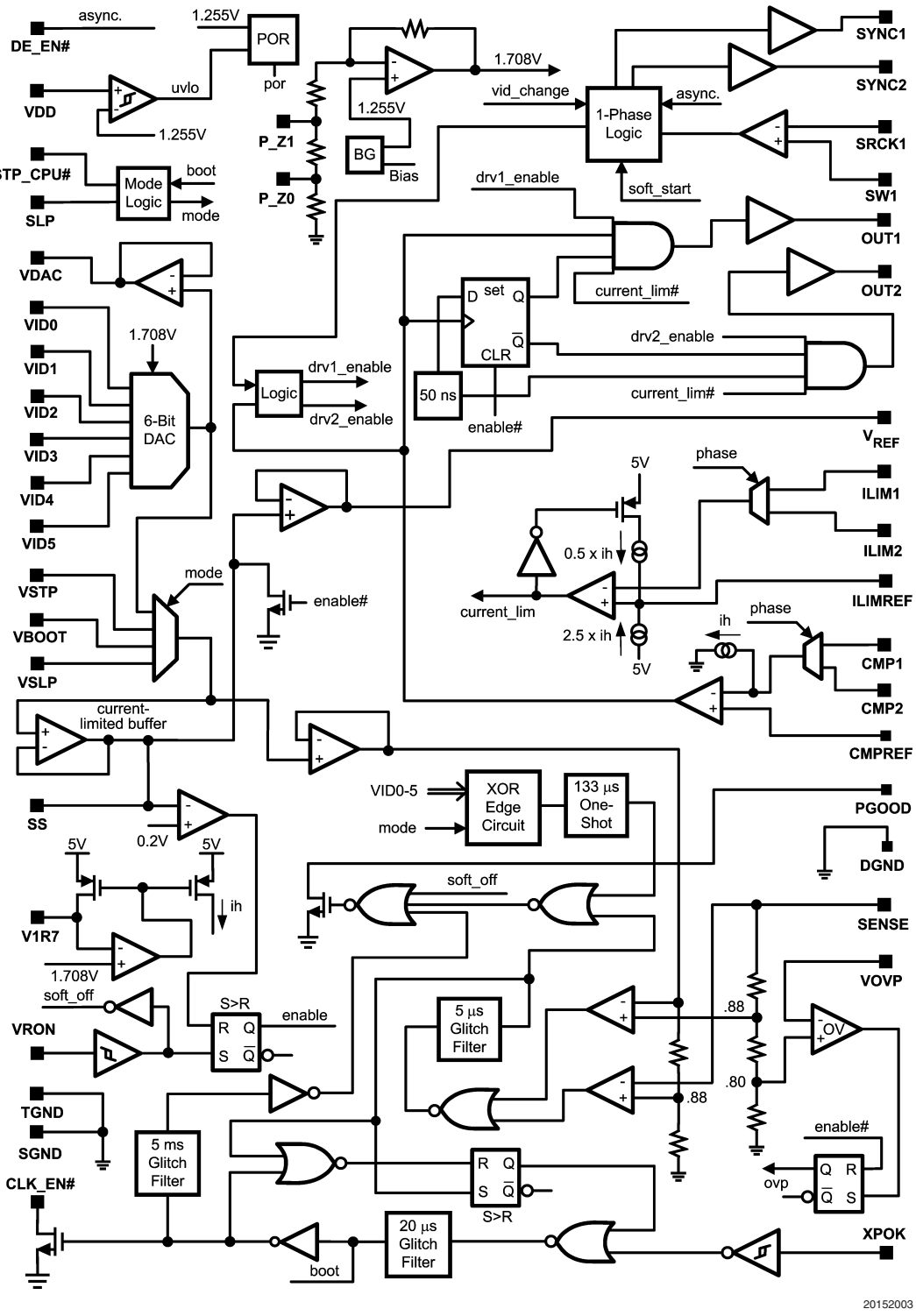
Note 4: For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Note 5: All limits are guaranteed at room temperature (standard face type) and at temperature extremes (bold face type). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Timing Diagram



Block Diagram



Operation Description

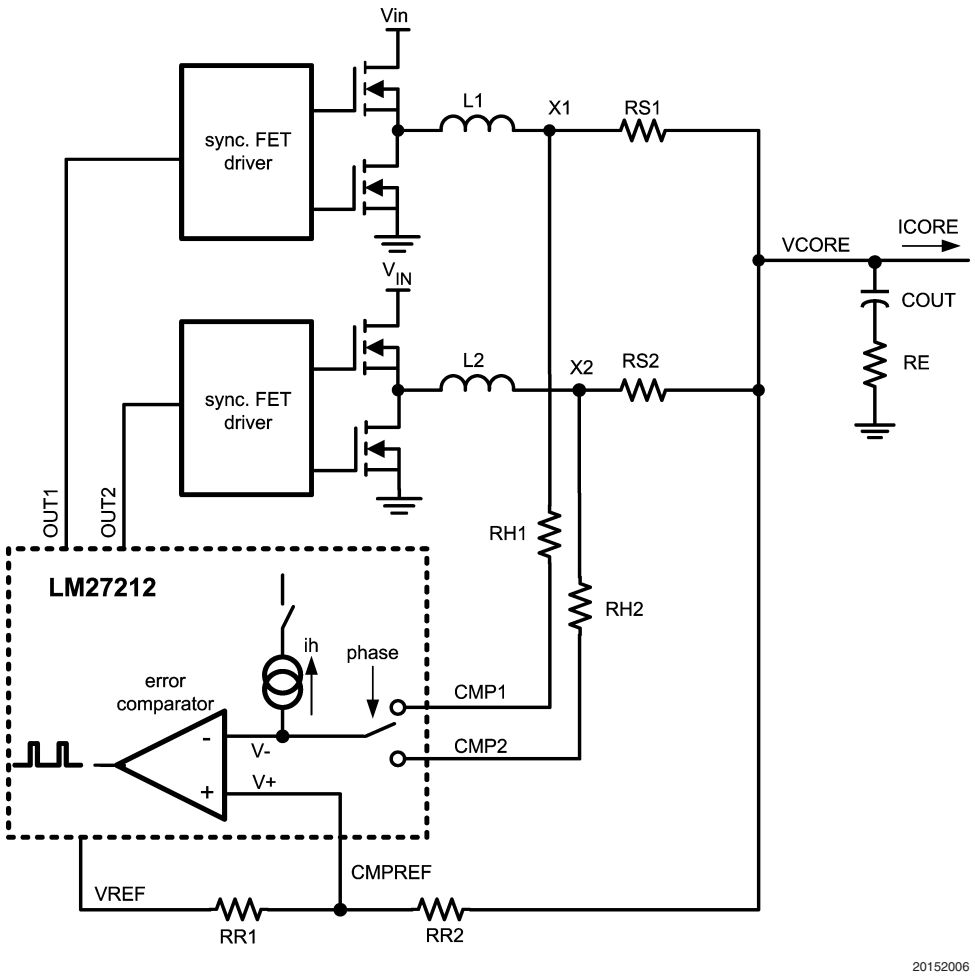


FIGURE 1. Two-Phase Current-Mode Hysteretic Operation

GENERAL

The LM27212 is a 2-phase current-mode hysteretic buck regulator controller that meets modern mobile CPU power requirements.

The LM27212 operates from a 5V supply and generates two logic signals that can be used to control external MOSFET drivers. The IC also has two pins (SYNC1 & SYNC2) that can be used to instruct the external MOSFET drivers to run synchronous or asynchronous, a feature to enable power saving operation in Stop CPU or Sleep mode.

CONTROL LOOP

Refer to *Figure 1*. The core of the control circuit is the error comparator, which turns off the top switch of a channel when that channel's peak inductor current exceeds the current command. The comparator turns on the top switch of the other channel when the previous channel's inductor current has dropped from its peak value by the preset hysteresis. By doing this the two channels are turned on and off alternately with a theoretical phase shift of 180 degrees.

To understand how the current mode works in this topology, let us assume the hysteresis current (ih) is zero, and the regulator can switch at infinite frequency. For channel 1, since it is switching at infinite frequency, the V- voltage is always equal to V+ voltage. Since the hysteresis current, ih is zero, V- is always equal to X1. Therefore the voltage across RS1 is always equal to that across RR2. In other words, inductor current in each channel is proportional to the voltage across RR2. So whenever there is a change in VCORE, there will be a corresponding but smaller change in RR2 voltage, which causes a finite change in the inductor currents. That is how load line programming is achieved.

In reality, the switching frequency is typically a few hundred kilohertz. The inductor currents therefore has a finite amount of ripple. The LM27212 sets the inductor ripple current by alternately forcing a hysteresis current (ih) through RH1 and RH2. The hysteresis current ih causes a hysteresis voltage across RH1 and RH2. When CMP1 gets connected to V- node of the error comparator via the internal mux, ih is turned on and flows through the RH1 resistor, establishing a hysteresis voltage across it. The error comparator trips when V- exceeds V+, at which moment X1 exceeds V+ by the hysteresis voltage. In other words, roughly half of the ripple voltage developed across RS1 is equal to the hysteresis voltage across RH1. After the error comparator trips, the top switch of Channel 1 is turned off, ih is turned off and L1's current starts to decrease. When L1's current droops to a

Operation Description (Continued)

point where X1 (which is now the same as V- because ih is zero) is equal to V+, Channel 2's top switch gets turned on and ih starts to flow through RH2.

In reality, the steady-state voltage across RR2 is not pure DC. That complicates the precise calculation of the operating point. See Design Considerations.

SOFT-START

By charging up the capacitor connected between the SS pin and ground with a 20µA current, the VREF pin voltage gradually and linearly increases. That causes the inductor current to build up, and hence the output voltage will follow VREF. The required capacitance at the SS pin is simply 20µA divided by the desired output voltage slew rate. For example, if output voltage needs to go to 1V within 2ms, then the capacitance required would be about 40nF.

SOFT SHUTDOWN

The LM27212 goes through a soft shutdown process upon receiving a de-asserted VRON signal. A constant 40µA current discharges the soft start capacitor and linearly brings down the VREF voltage. The output voltage will follow VREF until VREF is 0.2V, after which the bottom FET is kept on and the top FET is kept off, causing the output voltage to quickly drop to zero.

Soft shutdown serves two purposes. One is to prevent a severe negative output voltage while discharging the output capacitors during shutdown. The other is so that output voltage ramps down in a well controlled manner and the difference between various voltage rails supplying the processor can be controlled.

OVER-VOLTAGE PROTECTION

The over-voltage protection trigger level can be set by tying the VOVP pin to a constant voltage. When the output voltage exceeds the VOVP pin voltage by 25%, the IC will turn off the top FET and turn on the bottom FET. The soft start capacitor will be discharged by the soft shutdown current.

After the VDD pin voltage or VRON is toggled, the IC will go through a normal soft start.

POWER GOOD FLAG

After the EXT PWRGD signal is asserted at the XPOK pin, the LM27212 will wait 6ms and then release PGOOD if the core voltage is within ±12% of the initial VREF target voltage (VBOOT voltage).

During a Dynamic VID or a mode transition, the PGOOD is masked for about 130µs and asserted high.

Upon de-assertion of VRON, PGOOD is pulled low within 90ns.

DYNAMIC VID TRANSITIONS

Upon detecting a DAC code change, the LM27212 will blank the Power Good for about 130µs, during which time the VREF voltage gradually transitions to the new DAC voltage. The speed of the transition depends on the soft start capacitor. The current that charges or discharges the soft start capacitor during such a transition is 350µA typical. The slew rate of the Dynamic VID change is simply 350µA divided by SS pin capacitance. For example, if the soft start capacitor is 22nF, then the Dynamic VID slew rate is 16mV/µs.

DIODE EMULATION MODE

In such a mode, the zero-cross detector senses the Vds of the Channel 1 bottom FET while OUT1 is low. If the sensed Vds is negative, the bottom FET will remain on. If the sensed Vds starts to go positive, the bottom FET will be turend off so that inductor current cannot go negative. This action prevents energy from cycling back from output capacitors to the power source. This mode enjoys better efficiency than the pure asynchronous mode because before the inductor current goes to zero it flows through FET instead of a diode. By implementing such a mode, the switching frequency can drop significantly at light loads. As a result, both the switching loss and MOSFET gate charge loss can be significantly reduced.

STOP CPU MODE

During normal operation, if the STP_CPU# pin is asserted and the SLP pin is not asserted, the VREF pin voltage will transition to the voltage at the VSTP pin. The speed of the transition depends on the soft start capacitor. The current that charges or discharges the soft start capacitor during such a transition is 350µA typical. The slew rate of the mode change is simply 350µA divided by SS pin capacitance. For example, if the soft start capacitor is 22nF, then the output voltage slew rate is 16mV/µs. Whenever the LM27212 is entering or exiting the Stop CPU mode, PGOOD is masked for about 130µs.

SLEEP MODE

The LM27212 will enter the Sleep mode only when both STP_CPU# and SLP are asserted. Upon assertion of the Sleep mode, the VREF pin voltage will transition to the voltage at the VSLP pin. The speed of the transition depends on the soft start capacitor. The current that charges or discharges the soft start capacitor during such a transition is 350µA typical. The slew rate of the mode change is simply 350µA divided by SS pin capacitance. For example, if the soft start capacitor is 22nF, then the output voltage slew rate is 16mV/µs. Whenever the LM27212 is entering or exiting the Sleep mode, PGOOD is masked for about 130µs.

MODE CHANGE

A mode change is a change in the VREF voltage caused by entering or existing Stop CPU mode or Sleep mode. During mode change or a Dynamic VID event, the soft start capacitor is charged or discharged with a 350µA current.

POWER SAVING MODE

When both the DE_EN# and STP_CPU# pins are asserted and SLP is not toggling, the LM27212 will enter the Power Saving mode. In such a mode, Channel 1 will operate in Diode Emulator mode. Channel 2's status depends on SLP. If SLP is also asserted, Channel 2 will be turned off (both OUT2 and SYNC2 will remain low, i.e. all Channel 2 FETs will be off), and Vcore will go to the VSLP voltage. If SLP is not asserted, Channel 2 will operate in pure asynchronous mode in which the bottom FET will not be turned on, and Vcore will be VID value minus the Stop CPU offset.

If SLP goes from low to high during Power Saving mode, the LM27212 enforces two-channel synchronous mode for about 130µs to guarantee Vcore can be pulled down within the specified time. Refer to the Modes During Normal Operation table.

Operation Description (Continued)

Modes During Normal Operation

SLP	STP_CPU#	DE_EN#	Mode Description
0	0	0	Ch1 = DEM Ch2 = Asynch. Vcore = VID - offset
0	0	1	2-ph, Synch. Vcore = VID - offset
0	1	0	2-ph, Synch. Vcore = VID
0	1	1	
1	0	0	Ch1 = DEM Ch2 = off Vcore = VSLP
1	0	1	2-ph, Synch. Vcore = VSLP
1	1	0	
1	1	1	

Note:
1. DEM stands for Diode Emulator Mode.
2. Only for a transition from 000 to 100, a 130µs 2-phase operation is enforced.

CURRENT SHARING

Current sharing is guaranteed by actively sensing the inductor current in each channel and comparing the peak of each sensed current with the same reference. In a current mode hysteretic controller such as the LM27212, current sharing is intrinsic. However, due to the low resistance value of the sense resistors (as low as 1mΩ), care should be exercised to make sure that the layout of the sense resistors is symmetrical, especially how the sense lines are connected to the sense resistors.

CURRENT LIMITING

An adjustable current limit is built in. An internal current flowing from the ILIMREF pin to the output through a resistor establishes a voltage which is compared with the voltage across the sense resistors to determine whether the sense resistors are conducting too much current.

When the peak inductor current in Channel 1 exceeds the preset limit, the OUT1 pin will go low, causing the inductor current to drop. When the inductor current drops by an amount that corresponds to the hysteresis of the current limit, the OUT2 pin will be allowed to go high. If the inductor current of Channel 2 also hits current limit, then OUT2 pin will go low and so Channel 2 current will fall. When Channel 2 current falls by an amount that corresponds to current limit hysteresis, the OUT1 pin is allowed to go high again.

In the case of a persistent over current, the output voltage will continue to droop until the load current is equal to the current limit value. If the output voltage droops too much (12% below nominal), PGOOD will be de-asserted and the system may use that to de-assert VRON and thus shut down the regulator.

Design Considerations

NOMENCLATURE

ESR – Equivalent Series Resistance;

ESL - Equivalent Series Inductance;

Loading transient – a load transient when the load current goes from minimum load to full load;

Unloading transient – a load transient when the load current goes from full load to minimum load;

C_{min} – minimum allowed output capacitance;

C_{max} – maximum allowed output capacitance;

D – duty cycle;

f – switching frequency;

r – load line slope, e.g. -3mV/A or -3mΩ;

ΔV_{c_s} – maximum allowed output voltage excursion during a load transient, as derived from load device specifications;

ΔI_{c_s} – maximum load current change, as specified by the load device manufacturer;

V_{rip} – peak-to-peak output voltage ripple;

GENERAL

Due to the large and ultra-fast load transient behavior in modern digital devices, it is typically easier to start the design process with the output capacitors.

SWITCHING FREQUENCY RANGE

In a current-mode hysteretic controller such as the LM27212, switching frequency can be rather complicated to calculate. If we assume that the ESR zero frequency is much lower than the typical switching frequency (typically true for non-MLCs), the switching frequency can be determined from the following equation (refer to *Figure 1*):

$$f = \frac{(S_4 - S_2) \times (1 - 2D)}{(S_3 - S_1 + S_4 - S_2) \times \tau + ih \times RH1} \times \frac{1}{2}$$

Where

$$S_1 = \frac{RR1}{RR1 + RR2} \times \frac{R_e}{L} \times (V_{in} - 2 \times V_{out})$$

$$S_2 = \frac{RR1}{RR1 + RR2} \times \frac{R_e}{L} \times (2 \times V_{out})$$

$$S_3 = (R_e + RS1) \times \frac{V_{in} - V_{out}}{L} - R_e \times \frac{V_{out}}{L}$$

$$S_3 = (R_e + RS1) \times \frac{V_{in} - V_{out}}{L} - R_e \times \frac{V_{out}}{L}$$

$$S_4 = (2R_e + RS1) \times \frac{V_{out}}{L}$$

$$D = \frac{(R_{ds2} + RS1 + R_{dc} - |r|) \times \frac{I_{out}}{2} + V_{ref}}{V_{in} + (R_{ds2} - R_{ds1}) \times \frac{I_{out}}{2}}$$

Design Considerations (Continued)

$$V_{out} = V_{ref} + I_{out} \times r$$

In the equations, τ is the delay from error comparator trip point to the instant external power FETs start to switch. For the LM27212 and LM27222, that value is found to be 150ns typical.

To determine the maximum switching frequency, first use the following equation to find the V_{in} value where the frequency peaks (notice that maximum switching frequency happens at maximum V_{out} value.):

$$V_{in\_fmax} = 2 \times V_{out\_max} + \sqrt{4 \times V^2_{out\_max} + \frac{2 \times ih \times RH1 \times L}{R_e + RS1 - \frac{RR1 \times R_e}{RR1 + RR2}} \times \frac{V_{out\_max}}{\tau}}$$

Then calculate the frequency using V_{in_fmax} for V_{in}, and V_{out_max} for V_{out}.

Example: RR1 = RR2, Re = 3mΩ, L = 0.6µH, maximum V_{out} = 1.356V, maximum V_{in} = 8.4V, minimum V_{out} = 0.84V, RS1 = 3mΩ, Rds1 = 10mΩ, Rds2 = 4mΩ, I_{out} = 0A, r = -3mΩ, ih = 100µA, RH1 = 40Ω.

So V_{in_fmax} = 6.83V and maximum switching frequency is f_{max} = 350kHz

Lowest switching frequency happens at minimum V_{out} and maximum V_{in}.

So for the above example, f_{min} = 250kHz.

OUTPUT CAPACITORS

Output capacitors are critical in controlling the output voltage excursion when a load transient first happens. The initial voltage excursion consists of two portions, that caused by the output capacitor ESR, and that caused by the total capacitance. When the ESR value is close to the load line slope value, the initial voltage excursion will be dominated by the ESR. Otherwise, it will be mainly caused by loss of charge in the capacitors. For a load transient tutorial, please refer to the Output Capacitor Selection section in the LM2633 datasheet.

It is apparent that the ESR should not exceed the load line slope |r|, or the load device's specification will immediately be violated. In addition, the output capacitance should be greater than a minimum value which is required by the worst-case unloading transient.

$$C_{min} = \frac{\frac{L}{2} \times \left[\Delta V_{c\_s} - \sqrt{(\Delta V_{c\_s})^2 - (\Delta I_{c\_s} \times R_e)^2}\right]}{V_{out} \times R_e^2}$$

where

$$\Delta V_{c\_s} = |r| \times \Delta I_{c\_s} + \delta - \frac{1}{2} \times V_{rip}$$

Example 1: L = 0.6µH, ΔI_{c_s} = 20A, R_e = 3mΩ, V_{out} = 1.356V, r = -3mΩ, δ = 10mV, V_{rip} = 12mV.

The calculated ΔV_{c_s} = 64mV

The calculated minimum output capacitance is C_{min} = 1026µF.

Example 2: L = 0.2µH, ΔI_{c_s} = 20A, R_e = 0.125mΩ, V_{out} = 1.00V, r = -3mΩ, δ = 10mV, V_{rip} = 12mV

The calculated ΔV_{c_s} = 64mV

The calculated minimum output capacitance is C_{min} = 313µF.

The above calculations are based on the assumption that when the worst-case unloading transient happens, the top FETs of the two channels immediately turn off. If that is not always the case, more capacitance is needed and a bench test is probably necessary to determine how much more is needed.

OUTPUT INDUCTOR SELECTION

Large output inductor values will need large output capacitor values, whereas smaller inductance will cause larger output ripple voltage. To meet the budget for output ripple voltage, we need to find out what the ripple current in the inductors is.

We know the peak-to-peak inductor current is:

$$\Delta i = \frac{V_{out}}{f \times L} \times (1 - D)$$

By plotting switching frequency curves, it is found that the largest ripple current happens at the highest V_{in} and V_{out}.

Example: RR1 = RR2, R_e = 3mΩ, L = 0.6µH, maximum V_{out} = 1.356V, maximum V_{in} = 15V, RS1 = 3mΩ, R_{ds1} = 10mΩ, R_{ds2} = 4mΩ, I_{out} = 0A, r = -3mΩ, ih = 100µA, RH1 = 40Ω.

The calculated frequency is f = 266kHz, and D = 0.09

So the peak-to-peak inductor current is Δi = 7.73A

Therefore the output peak-to-peak ripple voltage is 23.2mV.

MOSFET SELECTION

Bottom FET Selection

During normal operation, the bottom FET is turned on and off at almost zero voltage. So only conduction loss is present in the bottom FET. The bottom FET power loss peaks at the maximum input voltage and load current. The most important parameter when choosing the bottom FET is the on-resistance. The lower the on-resistance, the less the power loss. The equation for the maximum allowed on-resistance at room temperature for a given FET package, is:

$$R_{ds2\_max} = \frac{1}{I^2_{out\_max} \times \left(1 - \frac{V_{out}}{V_{in\_max}}\right)} \times \frac{T_{j\_max} - T_{a\_max}}{[1 + TC \times (T_{j\_max} - 25°C/W)] \times R_{\theta ja}}$$

where T_{j_max} is the maximum allowed junction temperature in the FET, T_{a_max} is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on-resistance which is typically 4000ppm/°C.

If the calculated on-resistance is smaller than the lowest value available, multiple FETs can be used in parallel. If the design criterion is to use the highest R_{ds} FET, then the R_{ds2_max} of a single FET can be increased due to reduced current. In the case of two FETs in parallel, multiply the

Design Considerations (Continued)

calculated on-resistance by 4 to obtain the on-resistance for each FET. In the case of more FETs, that number is the square of the number of FETs. Since efficiency is very important in most cases, having the lowest on-resistance is usually more important than fully utilizing the thermal capacity of the package. So it is probably better to find the lowest Rds FET first, and then determine how many are needed.

Example: T_{j_max} = 100˚C, T_{a_max} = 60˚C, $R_{\theta ja}$ = 60˚C/W, V_{in_max} = 15V, V_{out} = 1.356V, and I_{out_max} = 30A.

$$R_{ds2\_max} = \frac{1}{(30A)^2 \times \left(1 - \frac{1.356V}{15V}\right)} \times$$

$$\frac{100°C - 60°C}{[1 + 0.004/°C \times (100°C - 25°C)] \times 60°C/W}$$

$$= 0.63\ m\Omega$$

If four bottom FETs are to be used (2 per channel), the maximum on-resistance can be as high as 0.63mΩ x 16 = 10mΩ. Generally it will be better to use lower on-resistance FETs.

Top FET Selection

The top FET has two types of losses – switching losses and the conduction losses. The switching loss mainly consists of the crossover loss and the bottom diode reverse recovery loss. It is rather difficult to estimate the switching losses. A general starting point is to allot 60% of the top FET thermal capacity to switching loss. The best way to find out is still to test it on the bench. The equation for calculating the on-resistance of the top FET is thus:

$$R_{ds1\_max} = \frac{V_{in\_min}}{2.5 \times I_{out\_max}^2 \times V_{out}} \times$$

$$\frac{T_{j\_max} - T_{a\_max}}{[1 + TC \times (T_{j\_max} - 25°C/W)] \times R_{\theta ja}}$$

where T_{j_max} is the maximum allowed junction temperature in the FET, T_{a_max} is the maximum ambient temperature, $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET, and TC is the temperature coefficient of the on-resistance which is typically 4000ppm/˚C.

Example: T_{j_max} = 100˚C, T_{a_max} = 60˚C, $R_{\theta ja}$ = 60˚C/W, V_{in_min} = 8.1V, V_{out} = 1.356V, and I_{out_max} = 30A.

$$R_{ds1\_max} = \frac{8.1V}{2.5 \times (30A)^2 \times 1.356V} \times$$

$$\frac{100°C - 60°C}{[1 + 0.004/°C \times (100°C - 25°C)] \times 60°C/W}$$

$$= 1.35\ m\Omega$$

If four top FETs are to be used (2 per channel), the maximum on-resistance can be as high as 1.35mΩ x 16 = 21.6mΩ.

Since the switching loss usually increases with bigger FETs, choosing a top FET with a much smaller on-resistance sometimes may not yield a noticeably lower temperature rise and better efficiency.

INPUT CAPACITOR SELECTION

The fact that the two switching channels of the LM27212 are 180˚ out of phase will help reduce the RMS value of the ripple current seen by the input capacitors. That will help extend input capacitor life span and result in a more efficient system. In most application, the output voltage is rather low compared to the input voltage. The corresponding duty cycles are therefore less than 50%, which means there will be no overlapping between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current is therefore:

$$I_{in\_rrm} = I_{out\_max} \times \sqrt{D \times \left(\frac{1}{2} - D\right)}$$

Example: I_{out_max} = 30A, V_{in} = 8.1V to 15V, V_{out} = 1.356V

The closer D is to 0.25, the larger the result. So the D value that should be used in this example should be D = 1.356 / 8.1V = 0.167.

$$I_{in\_rrm} = 30A \times \sqrt{0.167 \times (0.5 - 0.167)} = 7.1A$$

If we use 10µF ceramic capacitors at the input and each can handle 1.5A of RMS ripple current, then we need 5 or 6 of these capacitors.

SOFT-START CAPACITOR

The capacitor connected between the SS pin and ground serves several purposes. Namely, soft start slew rate, soft shutdown slew rate, and Dynamic VID and Mode Change slew rates.

During soft-start, the current charging the SS capacitor is 20µA typical.

During soft shutdown, the current discharging the SS capacitor is 40µA typical.

During Dynamic VID and Mode Change, the current charging or discharging the SS capacitor is 350µA typical.

Usually the Dynamic VID and Mode Change slew rate is more critical than soft-start and soft shutdown slew rates. So when selecting SS capacitor value, priority should be assigned accordingly.

The equation used to determine the SS capacitor value is:

$$C_{ss} = \frac{I_{ss}}{dv/dt}$$

where I_{SS} is the current through the SS pin, and dv/dt is the slew rate required.

The equation used to determine the transition time for a given slew rate and SS capacitance is:

$$\Delta t = \frac{\Delta V \times C_{ss}}{I_{ss}}$$

where ΔV is the voltage difference between the initial value and the end-of-transition value.

Design Considerations (Continued)

Example: soft start time is preferred to be 1ms to 3ms, initial Vcore is 1.37V, and Dynamic VID / Mode Change slew rate is preferred to be no less than 5mV/µs.

So,

$$C_{ss} = \frac{350\ \mu A}{5\ mV/\mu s} = 70\ nF \approx 68\ nF$$

Double-checking the soft start time:

$$\Delta t = \frac{1.37V \times 68\ nF}{20\ \mu A} = 4.65\ ms$$

To make sure during Sleep entry PGOOD doesn't go low, SS voltage must hit the PGOOD window of the target voltage before the PGOOD mask timer expires (around 130 µs). The following equation can be used to establish the approximate value of the largest SS capacitor.

$$C_{max} = \frac{A}{\ln\left(\frac{B}{A \times \Delta_0 + B}\right)} \times t$$

where Δ_0 is the difference between VSLP (typically around 0.74V) and the SS-pin voltage immediately before the Sleep entry, and t is the time it tkaes to reach the VSLP voltage. A and B are coefficients that depend on temperature.

Temperature	A	B
Room	-240e-6	-145e-6
110˚C	-220e-6	-90e-6

It is found that the SS-pin sink current is the lowest at 110˚C over the temperature range of -5˚C to 110˚C.

SETTING VOVP, VBOOT, VSLP AND IH

Refer to the Typical Application circuit.

The hysteresis current ih used in the previous equations is equal to the current sourced by the V1R7 pin. So calculation of the R2, R3, R5 and R6 values is straightforward.

Example: hysteresis current ih = 100µA, Sleep voltage VSLP = 0.748V, initial start up voltage VBOOT = 1.37V, OVP threshold VOVP = 1.7V.

$$R_6 = \frac{VSLP}{ih} = \frac{0.748V}{100\ \mu A} = 7.48\ k\Omega \approx 7.50\ k\Omega$$

$$R_5 = \frac{VBOOT}{ih} - R_6 = \frac{1.37V}{100\ \mu A} - 7.50\ k\Omega$$

$$= 6.2\ k\Omega \approx 6.19\ k\Omega$$

$$R_3 = \frac{VOVP}{ih} - R_5 - R_6$$

$$= \frac{1.65V}{100\ \mu A} - 6.19\ k\Omega - 750\ k\Omega$$

$$= 2.81\ k\Omega \approx 2.80\ k\Omega$$

$$R_2 = \frac{V1R7}{ih} - R_3 - R_5 - R_6$$

$$= \frac{1.708V}{100\ \mu A} - 2.80\ k\Omega - 6.19\ k\Omega - 750\ k\Omega$$

$$= 590\Omega$$

SETTING STOP CPU VOLTAGE VSTP

Refer to Typical Application circuit.

The Stop CPU voltage VSTP is a certain percentage lower than the DAC output voltage. The equation used to determine the R7 resistor values is:

$$R_7 = \frac{\delta}{1 - \delta} \times R_8$$

where δ is the percentage VSTP is lower than VDAC.

Example: δ = -2.69%.

If we choose R8 = 100kΩ, then

$$R_7 = \frac{0.0269}{1 - 0.0269} \times 100\ k\Omega = 2.764\ k\Omega \approx 2.74\ k\Omega$$

Choosing too small an R8 will result in too much current draw from the VDD pin, hurting system efficiency. Too large an R8 value may result in noise issues.

SETTING THE HYSTERESIS

Refer to *Figure 1*. The hysteresis voltages across RH1 and RH2 contribute to switching frequency characteristics, inductor ripple current, noise immunity and line regulation. Typically the higher the hysteresis, the lower the switching frequency and the tighter the frequency range. Also the higher the hysteresis, the higher the ripple current. In a typical mobile CPU design, the hysteresis is typically set at a few milivolts.

Example: hysteresis voltage is set at 6mV, hysteresis current ih = 100µA

So RH1 = RH2 = 6mV ÷ 100µA = 60Ω.

Design Considerations (Continued)

SETTING CURRENT LIMIT

The current limit comparator compares the voltage pre-established across the current limit set resistor (R13 in *Figure 1*) and the voltage across the current sense resistors.

The current sourced by the ILIMREF pin is 3 times ih. The equation to determine R13 is:

$$R_{13} = \frac{I_{peak} \times RS1}{I_{ref}}$$

where I_{peak} is the maximum allowed peak inductor current, RS1 is the sense resistance and I_{ref} is the current sourced by the ILIMREF pin.

Example: RS1 = RS2 = 3mΩ, I_{peak} = 21A, I_{ref} = 300µA.

So R13 = 210Ω. Note I_{peak} is usually half of maximum output current plus inductor current ripple plus some margin. Suppose the maximum output current is 24A, and inductor ripple current is ±5A. So choosing an I_{peak} value of 21A gives us a margin of 8A in load current.

SETTING THE LOAD LINE SLOPE

Refer to *Figure 1*. In two-phase operation mode, the load line is set by the ratio between RR1 and RR2. The equation is:

$$\frac{RR2}{RR1 + RR2} = \frac{RS1}{2 \times |r|}$$

Example: RS1 = 3mΩ, r = -3mΩ.

So RR2 divided by RR1+RR2 is 0.5

It is suggested that the user choose the parallel combination of RR1 and RR2 to be close to RH1 or RH2 to cancel the DC offset caused by bias current of the CMPx pins. So if RH1 is 60Ω, then RR1 = RR2 = 120Ω.

Special PCB Layout Considerations

1. Grounding

There are two grounds, one is power ground, the other is signal ground. Power ground is the plane which DGND, power FETs, input and output capacitors are directly connected to. Signal ground is a separate plane that R6 / R8 / C3 / C7 and SGND / TGND (if LLP, also the thermal pad) are connected to. Signal ground should connect to the ground sense via through a trace.

PGND should connect to the source pins of Channel 1 bottom FETs through a separate trace. If vias have to be used during routing, make sure the vias are isolated from all ground planes, polygons and fills.

2. Sensing

The VCORE sense via should be as close to output bulk capacitors as possible and should be symmetrical with respect to the two phases. It should also be isolated from any VCORE planes / polygons / fills other than those on the top layer. The VCORE sense signal should be used for the SENSE pin, R13 and R14. This trace should be kept away from power inductors.

The ground sense via is the only place power ground connects to signal ground. The via should be as close to the output bulk capacitors as possible. It should be symmetrical with respect to the two phases. It should also be isolated from any ground planes/polygons/fills other than those on top layer. The control IC should be close to this Via.

SW1 sense needs a trace from the SW1 pin to the drain pins of the Channel 1 bottom FETs. If vias have to be used during routing, make sure the vias are isolated from all SW1 planes / polygons / fills. Keep the SW1 sense trace as close as possible to the SRCK1 trace.

Current sense vias should connect to the current sense resistor pads through a top layer trace. The vias should be isolated from all planes / polygons / fills on the same net but not on the top layer. They should connect to R11 / R12 and R18 / R19 through an isolated trace. Current sense traces should be kept away from power inductors.

Special PCB Layout Considerations (Continued)

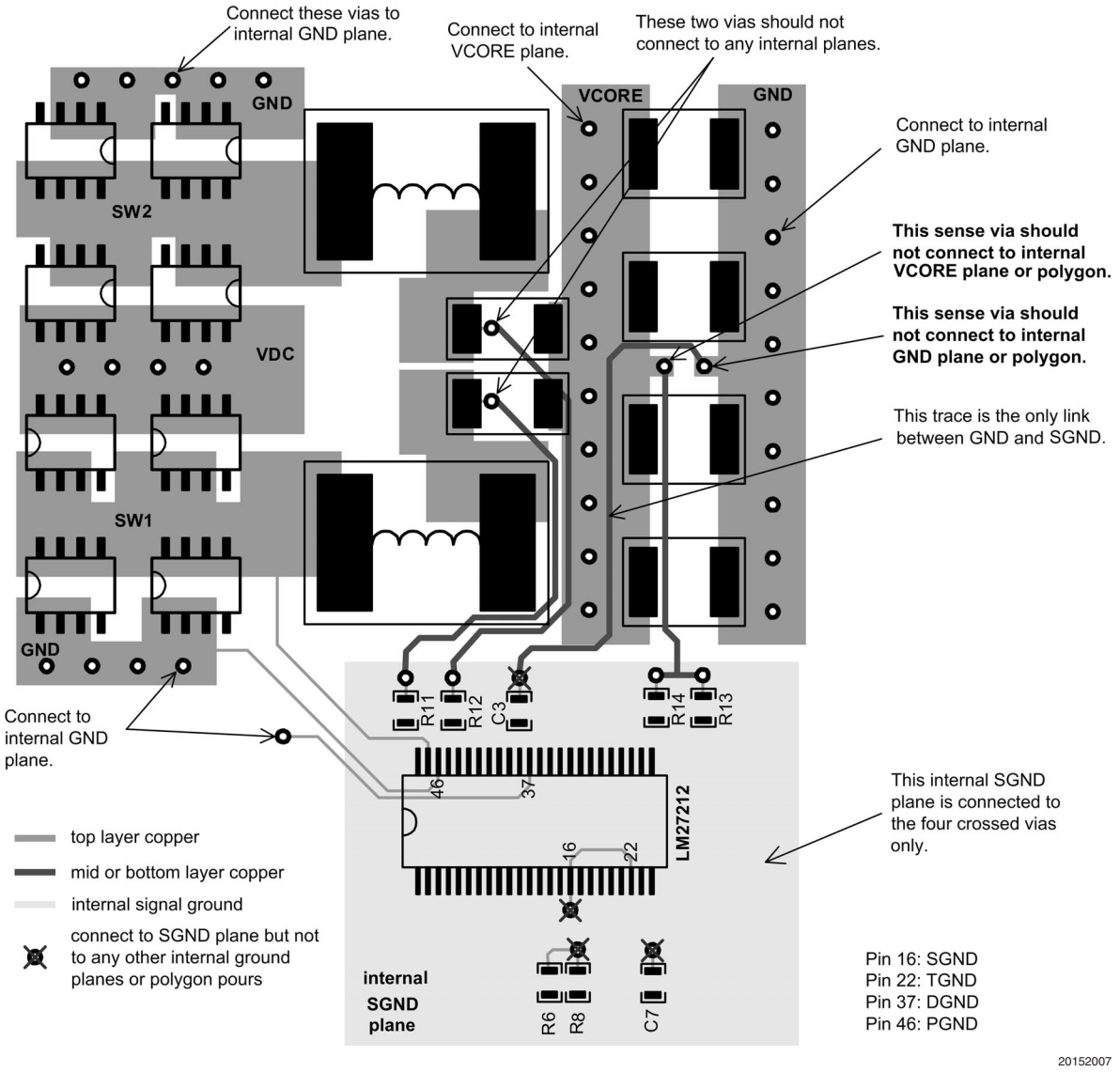
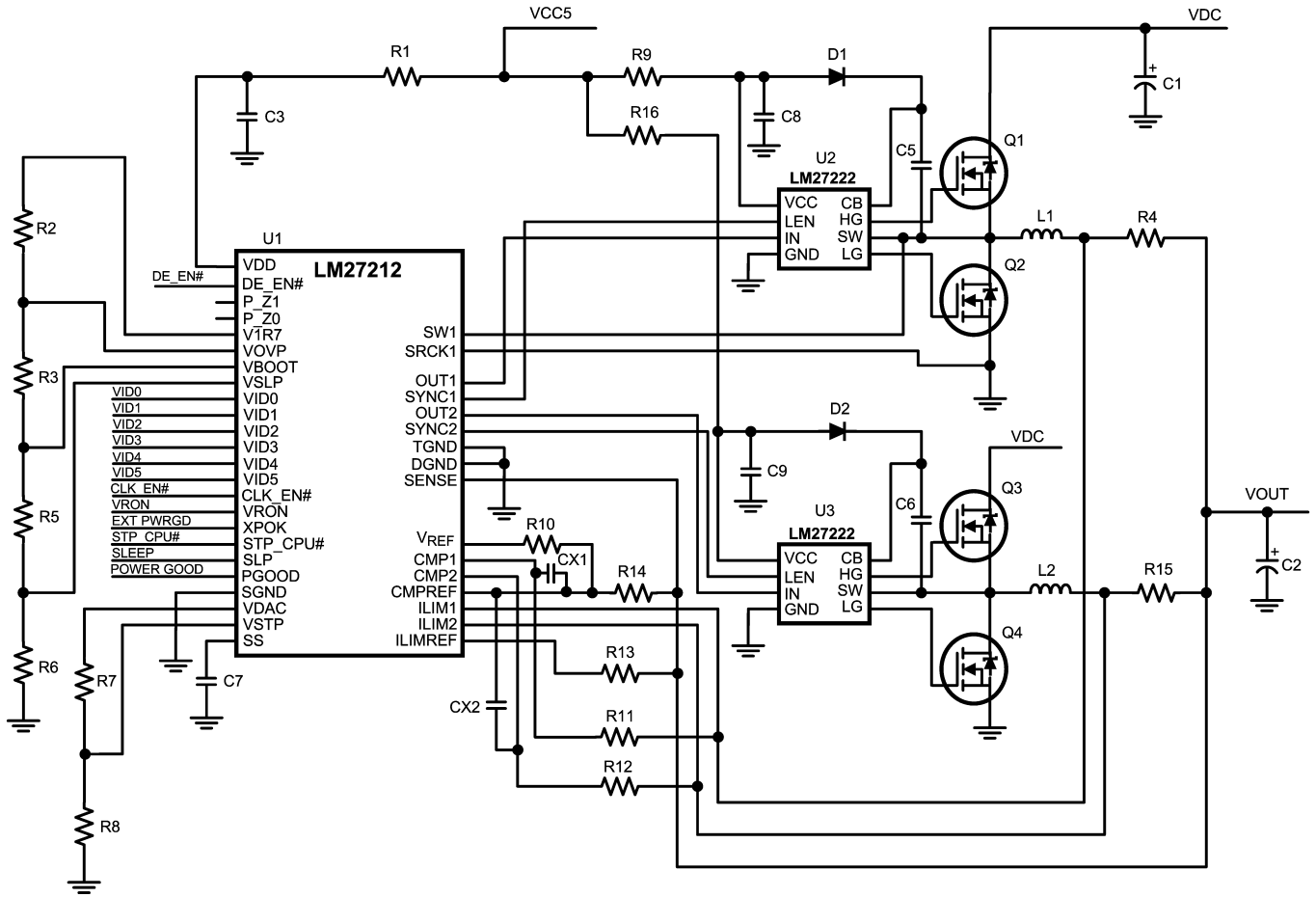


FIGURE 2. PCB Layout Example

Application Example



20152005

Bill of Materials Design 1

DESIGN 1. (VDC = 8.1V to 21V, IOUT = 32A continuous, Maximum Load Step = 24A)

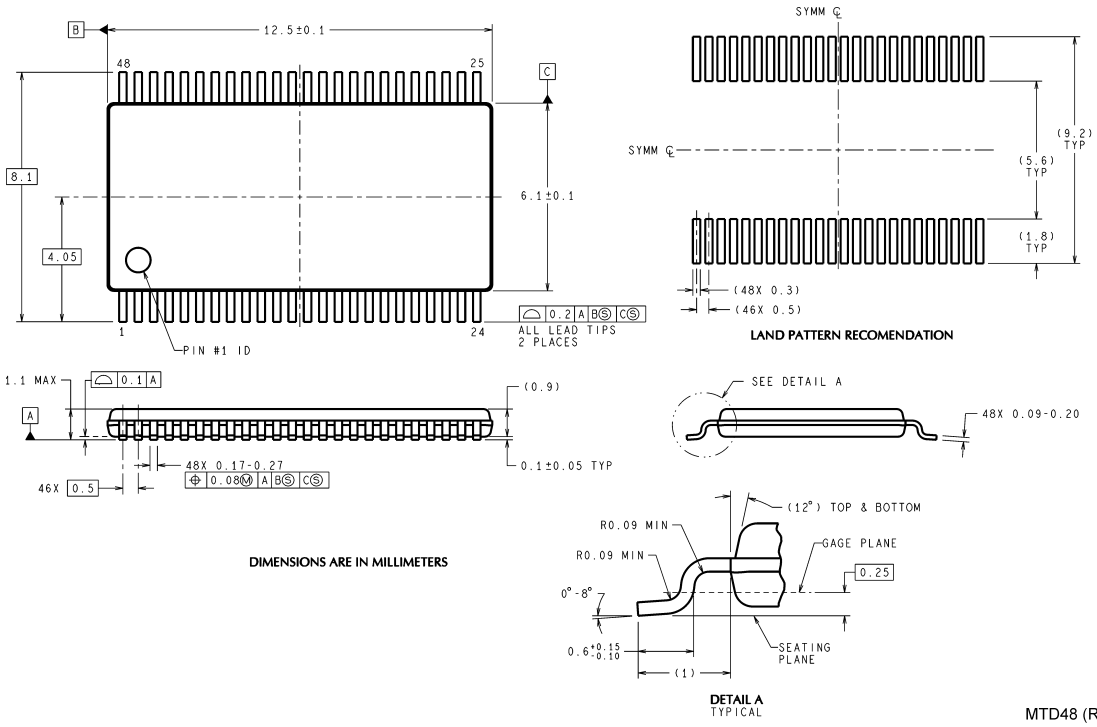
ID	Part Number	Type	Size	Parameters	Qt.	Vendor
C1	C4532X7R1E106M	CAPACITOR, MLC	1812	25V, 10µF, X7R	5	TDK
C2	6TPD330M	CAPACITOR, POSCAP	7.3X4.3X3.8 mm3	6.3V, 330µF, 10mΩ	4	SANYO
	EEFSD0E221R	CAPACITOR, SP	7.3X4.3X2.8 mm3	2.5V, 220µF, 7mΩ		PANSONIC
C3	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
C5	VJ0805Y154KXJ	CAPACITOR	0805	0.15µF, 16V, X7R	1	VISHAY
C6	VJ0805Y154KXJ	CAPACITOR	0805	0.15µF, 16V, X7R	1	VISHAY
C7	VJ0805Y223KXJ	CAPACITOR	0805	22nF, 16V, X7R	1	VISHAY
C8	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
C9	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
CX1	VJ0805Y122KXJ	CAPACITOR	0805	1.2nF, 16V, X7R	1	VISHAY
CX2	VJ0805Y122KXJ	CAPACITOR	0805	1.2nF, 16V, X7R	1	VISHAY
CX3	VJ0805Y471KXJ	CAPACITOR	0805	470pF, 16V, X7R	1	VISHAY
CX4	VJ0805Y471KXJ	CAPACITOR	0805	470pF, 16V, X7R	1	VISHAY
D1	BAT54LT1	DIODE, SCHOTKY	SOT-23	30V	1	MOTOROLA
D2	BAT54LT1	DIODE, SCHOTKY	SOT-23	30V	1	MOTOROLA
D3	MBRS130LT3	DIODE, SCHOTKY	SMB	30V, 1A	1	MOTOROLA
D4	MBRS130LT3	DIODE, SCHOTKY	SMB	30V, 1A	1	MOTOROLA
L1	ETQP1H0R6BFA	INDUCTOR	13X12.9X6 mm3	0.56µH@26A, 0.9mΩ	1	PANASONIC
L2	ETQP1H0R6BFA	INDUCTOR	13X12.9X6 mm3	0.56µH@26A, 0.9mΩ	1	PANASONIC
Q1	Si4892DY	MOSFET, N-TYPE	SO-8	30V, 8.7nC, 20mΩ@4.5V	2	VISHAY
Q2	Si4362DY	MOSFET, N-TYPE	SO-8	30V, 40nC, 6.3mΩ@4.5V	2	VISHAY
Q3	Si4892DY	MOSFET, N-TYPE	SO-8	30V, 8.7nC, 20mΩ@4.5V	2	VISHAY
Q4	Si4362DY	MOSFET, N-TYPE	SO-8	30V, 40nC, 6.3mΩ@4.5V	2	VISHAY
R1		RESISTOR	0805	33Ω	1	VISHAY
R2		RESISTOR	0805	0Ω	1	VISHAY
R3		RESISTOR	0805	5.11kΩ, ±1%	1	VISHAY
R4	WSL2512	RESISTOR, SENSE	2512	3mΩ, 1W@70˚C, ±1%, < 2.5mm Tall	1	VISHAY
R5		RESISTOR	0805	4.53kΩ, ±1%	1	VISHAY
R6		RESISTOR	0805	7.50kΩ, ±1%	1	VISHAY
R7		RESISTOR	0805	1.21kΩ, ±1%	1	VISHAY
R8		RESISTOR	0805	100kΩ, ±1%	1	VISHAY
R9		RESISTOR	0805	1.5Ω, ±5%	1	VISHAY
R10		RESISTOR	0805	121Ω, ±1%	1	VISHAY
R11		RESISTOR	0805	60.4Ω, ±1%	1	VISHAY
R12		RESISTOR	0805	60.4Ω, ±1%	1	VISHAY
R13		RESISTOR	0805	200Ω, ±1%	1	VISHAY
R14		RESISTOR	0805	121Ω, ±1%	1	VISHAY
R15	WSL2512	RESISTOR, SENSE	2512	3mΩ, 1W@70˚C, ±1%, < 2.5mm Tall	1	VISHAY
R16		RESISTOR	0805	1.5Ω, ±5%	1	VISHAY
R17		RESISTOR	0805	200Ω, ±1%	1	VISHAY
R18		RESISTOR	0805	200Ω, ±1%	1	VISHAY
U1	LM27212	CONTROLLER, HYSTERETIC	TSSOP-48 or LLP-48	2-Phase	1	NSC
U2	LM27222	DRIVER	SO-8 or LLP-8	30V, 4.5A	1	NSC
U3	LM27222	DRIVER	SO-8 or LLP-8	30V, 4.5A	1	NSC

Bill of Materials Design 2

DESIGN 2. (VDC = 8.1V to 21V, IOUT = 25A continuous, Maximum Load Step = 18.6A)

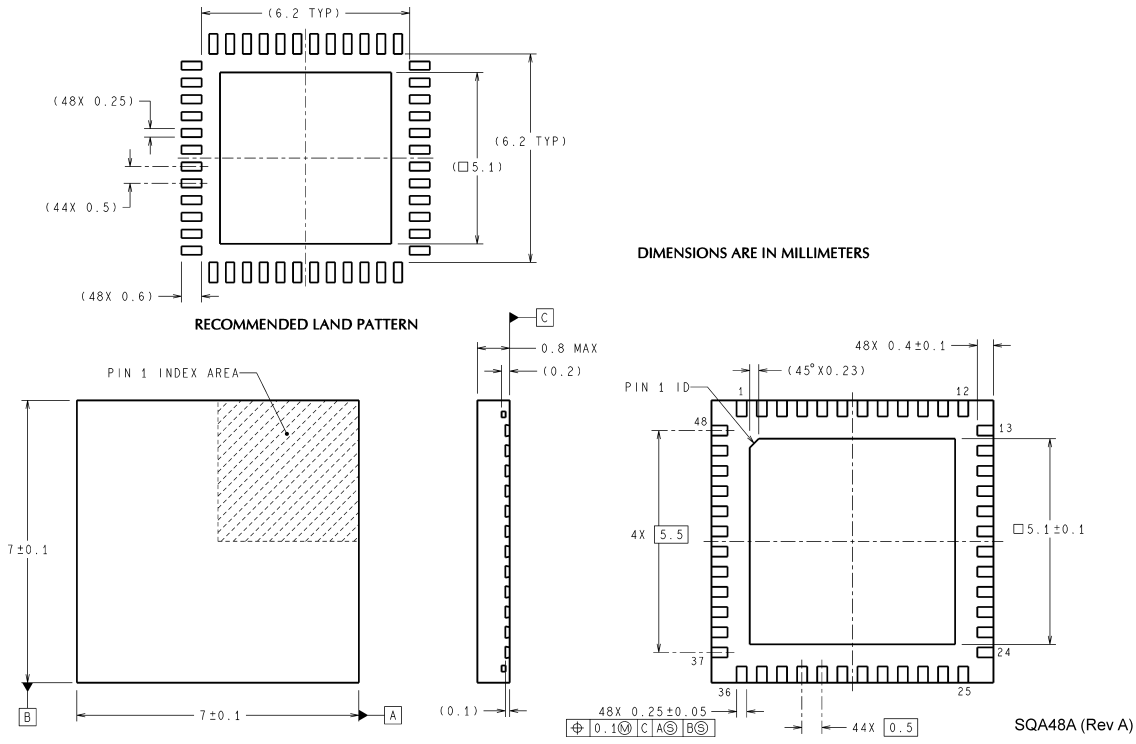
ID	Part Number	Type	Size	Parameters	Qt.	Vendor
C1	C4532X7R1E106M	CAPACITOR, MLC	1812	25V, 10µF, X7R	4	TDK
C2	6TPD330M	CAPACITOR, POSCAP	7.3X4.3X3.8 mm3	6.3V, 330µF, 10mΩ	3	SANYO
	EEFSD0E221R	CAPACITOR, SP	7.3X4.3X2.8 mm3	2.5V, 220µF, 7mΩ		PANSONIC
C3	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
C5	VJ0805Y154KXJ	CAPACITOR	0805	0.15µF, 16V, X7R	1	VISHAY
C6	VJ0805Y154KXJ	CAPACITOR	0805	0.15µF, 16V, X7R	1	VISHAY
C7	VJ0805Y223KXJ	CAPACITOR	0805	22nF, 16V, X7R	1	VISHAY
C8	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
C9	VJ0805Y105KXJ	CAPACITOR	0805	1µF, 16V, X7R	1	VISHAY
CX1	VJ0805Y122KXJ	CAPACITOR	0805	1.2nF, 16V, X7R	1	VISHAY
CX2	VJ0805Y122KXJ	CAPACITOR	0805	1.2nF, 16V, X7R	1	VISHAY
CX3	VJ0805Y471KXJ	CAPACITOR	0805	470pF, 16V, X7R	1	VISHAY
CX4	VJ0805Y471KXJ	CAPACITOR	0805	470pF, 16V, X7R	1	VISHAY
D1	BAT54LT1	DIODE, SCHOTKY	SOT-23	30V	1	MOTOROLA
D2	BAT54LT1	DIODE, SCHOTKY	SOT-23	30V	1	MOTOROLA
D3	MBRS130LT3	DIODE, SCHOTKY	SMB	30V, 1A	1	MOTOROLA
D4	MBRS130LT3	DIODE, SCHOTKY	SMB	30V, 1A	1	MOTOROLA
L1	ETQP1H0R6BFA	INDUCTOR	13X12.9X6 mm3	0.56µH@26A, 0.9mΩ	1	PANASONIC
L2	ETQP1H0R6BFA	INDUCTOR	13X12.9X6 mm3	0.56µH@26A, 0.9mΩ	1	PANASONIC
Q1	Si4892DY	MOSFET, N-TYPE	SO-8	30V, 8.7nC, 20mΩ@4.5V	1	VISHAY
Q2	Si4362DY	MOSFET, N-TYPE	SO-8	30V, 40nC, 6.3mΩ@4.5V	2	VISHAY
Q3	Si4892DY	MOSFET, N-TYPE	SO-8	30V, 8.7nC, 20mΩ@4.5V	1	VISHAY
Q4	Si4362DY	MOSFET, N-TYPE	SO-8	30V, 40nC, 6.3mΩ@4.5V	2	VISHAY
R1		RESISTOR	0805	33Ω	1	VISHAY
R2		RESISTOR	0805	0Ω	1	VISHAY
R3		RESISTOR	0805	5.11kΩ, ±1%	1	VISHAY
R4	WSL2512	RESISTOR, SENSE	2512	3mΩ, 1W@70˚C, ±1%, < 2.5mm Tall	1	VISHAY
R5		RESISTOR	0805	4.53kΩ, ±1%	1	VISHAY
R6		RESISTOR	0805	7.50kΩ, ±1%	1	VISHAY
R7		RESISTOR	0805	1.21kΩ, ±1%	1	VISHAY
R8		RESISTOR	0805	100kΩ, ±1%	1	VISHAY
R9		RESISTOR	0805	1.5Ω, ±5%	1	VISHAY
R10		RESISTOR	0805	121Ω, ±1%	1	VISHAY
R11		RESISTOR	0805	60.4Ω, ±1%	1	VISHAY
R12		RESISTOR	0805	60.4Ω, ±1%	1	VISHAY
R13		RESISTOR	0805	200Ω, ±1%	1	VISHAY
R14		RESISTOR	0805	121Ω, ±1%	1	VISHAY
R15	WSL2512	RESISTOR, SENSE	2512	3mΩ, 1W@70˚C, ±1%, < 2.5mm Tall	1	VISHAY
R16		RESISTOR	0805	1.5Ω, ±5%	1	VISHAY
R17		RESISTOR	0805	200Ω, ±1%	1	VISHAY
R18		RESISTOR	0805	200Ω, ±1%	1	VISHAY
U1	LM27212	CONTROLLER, HYSTERETIC	TSSOP-48 or LLP-48	2-Phase	1	NSC
U2	LM27222	DRIVER	SO-8 or LLP-8	30V, 4.5A	1	NSC
U3	LM27222	DRIVER	SO-8 or LLP-8	30V, 4.5A	1	NSC

Physical Dimensions inches (millimeters) unless otherwise noted



MTD48 (Rev E)

48-Lead TSSOP Package
Order Number LM27212MTD
NS Package Number MTD48



SQA48A (Rev A)

48-Lead LLP Package
Order Number LM27212SQ
NS Package Number SQA48A

Notes

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